Gedächtnisprotokoll SoC Oral Exam 26.07.2022

1. How does a simple Latch keep ist data?
2. What is Metastability?
3. What is the difference between Waterfall and Spiral Development?
4. What is the difference between Describe&Synthesize and Platform Design Approach?
5. ARM Processor Architecture given, explain the signal flow for an ADD command.
6. What does single-layer and multi-layer bus structure mean?
7. Given a Timing Diagram of an AHB burst read. One signal had „?“ as name, what is it called (HRDATA). Explain why there was a BUSY state on HTRANS (master needed one cycle pause), explain what HREADY=0 does to the transmission (wait state on the bus initiated by the slave, no signal changes). Why is there a delay between Address sending and receiving the data? (Pipelining)
8. Is UART synchronous or asynchronous? (asynchronous)
9. Is UART differential or single-ended? (single-ended)
10. Given a diagram of a CAN Bus Frame. One bitfield missing a name (checksum).
11. Is CAN differential or single-ended? (differential)
12. Why do you use bit-stuffing on CAN Bus? (Synchronization purposes on the receiving end)
13. Why don’t you use bit-stuffing on UART? (Stop Bit synchronizes the Bus)
14. Why don’t you use bit-stuffing on SPI? (because it’s synchronous)